

# Am71/81LS95 • Am71/81LS96

# Am71/81LS97 • Am71/81LS98

## Three-State Octal Buffers

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus line directly
- Typical propagation delay  
Am71/81LS95, Am71/81LS97 13ns  
Am71/81LS96, Am71/81LS98 10ns
- Typical power dissipation  
Am71/81LS95, Am71/81LS97 80mW  
Am71/81LS96, Am71/81LS98 65mW
- PNP inputs reduce DC loading on bus lines
- Am71/81LS96 and Am71/81LS98 are inverting;  
Am71/81LS95 and Am71/81LS97 are non-inverting
- 20-pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

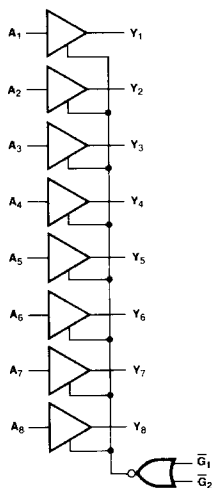
### GENERAL DESCRIPTION

The Am71/81LS95, Am71/81LS96, Am71/81LS97 and Am71/81LS98 are octal buffers fabricated using Advanced Low-Power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

The Am71/81LS95 and Am71/81LS97 present true data at the outputs, while the Am71/81LS96 and Am71/81LS98 are inverting. The Am71/81LS95 and Am71/81LS96 have a common enable for all eight buffers with access through a 2-input NOR gate. The Am71/81LS97 and Am71/81LS98 octal buffers have four buffers enabled from one common line, and the other four buffers enabled from another common line. In all cases the outputs are placed in the three-state condition by applying a high logic level to the enable pins. All parts feature low current PNP inputs.

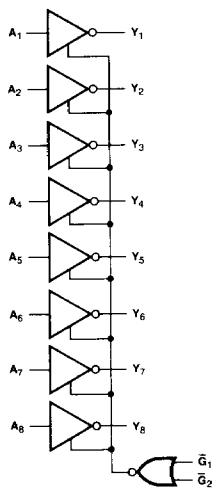
### LOGIC DIAGRAMS

Am71/81LS95



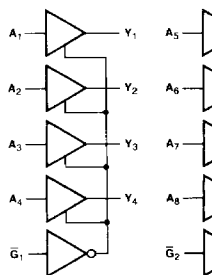
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Am71/81LS96



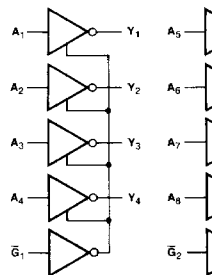
LIC-488

Am71/81LS97



LIC-489

Am71/81LS98



LIC-490

'LS95

INPUTS		OUTPUT Y	
$\bar{G}_1$	$\bar{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

'LS96

INPUTS		OUTPUT Y	
$\bar{G}_1$	$\bar{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

'LS97

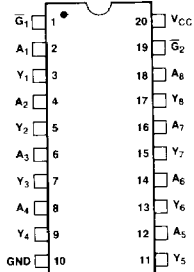
INPUTS	OUTPUT Y	
$\bar{G}$	A	Y
H	X	Z
L	H	Z
L	L	L

'LS98

INPUTS	OUTPUT Y	
$\bar{G}$	A	Y
H	X	Z
L	H	L
L	L	H

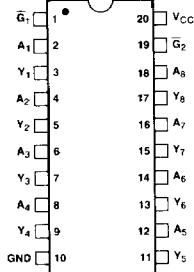
### CONNECTION DIAGRAMS — Top Views

Am71/81LS95



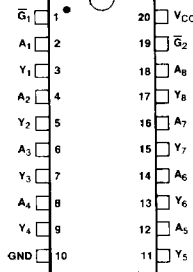
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Am71/81LS96



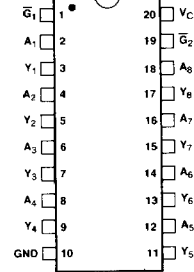
LIC-492

Am71/81LS97



LIC-493

Am71/81LS98



LIC-494

**MAXIMUM RATINGS** above which the useful life may be impaired

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	-0.5V to +V <sub>CC</sub> max.
DC Input Voltage	-0.5V to +7.0V
DC Output Current	150mA
DC Input Current	-30mA to +5.0mA

**ELECTRICAL CHARACTERISTICS**

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = 5.0V ± 5%	(MIN. = 4.75V MAX. = 5.25V)
MIL	T <sub>A</sub> = -55°C to +125°C	V <sub>CC</sub> = 5.0V ± 10%	(MIN. = 4.50V MAX. = 5.50V)

**Am71/81LS95****Am71/81LS96****Am71/81LS97****Am71/81LS98****DC CHARACTERISTICS OVER OPERATING RANGE**

Parameters		Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V <sub>IH</sub>		High Level Input Voltage			2			Volts
V <sub>IL</sub>		Low Level Input Voltage					0.8	Volts
V <sub>I</sub>		Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>I</sub> = -18mA				-1.5	Volts
I <sub>OH</sub>		High Level Output Current	MIL				-1.0	mA
			COM'L				-2.6	
V <sub>OH</sub>		High Level Output Voltage	V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.0V V <sub>IL</sub> = 0.8V	COM'L	I <sub>OH</sub> = -5.0mA	2.4		Volts
					I <sub>OH</sub> = -2.6mA	2.7		
				MIL, I <sub>OH</sub> = -1.0mA		2.5		
I <sub>OL</sub>		Low Level Output Current	COM'L				16	mA
			MIL				8	
V <sub>OL</sub>		Low Level Output Voltage	V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.0V V <sub>IL</sub> = 0.8V	COM'L, I <sub>OL</sub> = 16mA			0.5	V
				MIL, I <sub>OL</sub> = 8.0mA			0.4	
I <sub>O(OFF)</sub>		Off-State (High-Impedance State) Output Current	V <sub>CC</sub> = Max., V <sub>IH</sub> = 2.0V V <sub>IL</sub> = 0.8V	V <sub>O</sub> = 0.4V			-20	μA
				V <sub>O</sub> = 2.4V			20	
I <sub>I</sub>		Input Current at Maximum Input Voltage	V <sub>CC</sub> = Max., V <sub>I</sub> = 7.0V				0.1	mA
I <sub>IH</sub>		High Level Input Current	V <sub>CC</sub> = Max., V <sub>I</sub> = 2.7V				20	μA
I <sub>IL</sub>	Low Level Input Current	A Input	V <sub>CC</sub> = Max.	Both $\bar{G}$ Inputs at 2.0V	V <sub>I</sub> = 0.5V		-50	μA
		$\bar{G}$ Input		Both $\bar{G}$ Inputs at 0.4V	V <sub>I</sub> = 0.4V		-0.36	
					V <sub>I</sub> = 0.4V		-0.36	
I <sub>OS</sub>		Short Circuit Output Current	V <sub>CC</sub> = Max. (Note 2)		-30	-60	-130	mA
I <sub>CC</sub>		Supply Current	V <sub>CC</sub> = Max.	Am71/81LS95, Am71/81LS97		16	26	mA
				Am71/81LS96, Am71/81LS98		13	21	

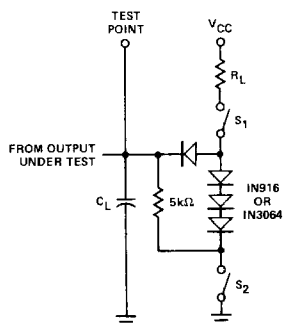
Notes: 1. All typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C.

2. Not more than output should be shorted at a time, and duration of the short circuit should not exceed one second.

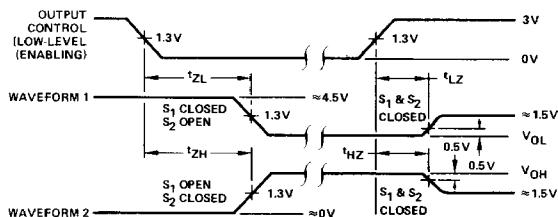
**SWITCHING CHARACTERISTICS** V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C**Am71/81LS95**  
**Am71/81LS97****Am71/81LS96**  
**Am71/81LS98**

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t <sub>PLH</sub>	Propagation Delay Time, Low-to-High Level Output	C <sub>L</sub> = 15pF, R <sub>L</sub> = 2kΩ			11	16		6	10	ns
t <sub>PHL</sub>	Propagation Delay Time, High-to-Low Level Output				15	22		13	17	ns
t <sub>ZH</sub>	Output Enable Time to High Level				16	25		17	27	ns
t <sub>ZL</sub>	Output Enable Time to Low Level				13	20		16	25	ns
t <sub>HZ</sub>	Output Disable Time from HIGH Level	C <sub>L</sub> = 5pF, R <sub>L</sub> = 2kΩ			13	20		13	20	ns
t <sub>LZ</sub>	Output Disable Time from Low Level				19	27		18	27	

## SWITCHING CHARACTERISTICS TEST CONDITIONS

LOAD CIRCUIT FOR  
THREE-STATE OUTPUTS

LIC-495

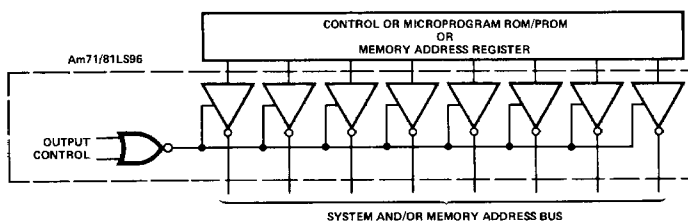
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

LIC-496

- Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.  
 4. Pulse generator characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_{OUT} \approx 50\Omega$ ,  $t_r \leq 15\text{ns}$ ,  $t_f \leq 6\text{ns}$ .  
 5. When measuring  $t_{PLH}$  and  $t_{PHL}$ , switches  $S_1$  and  $S_2$  are closed.

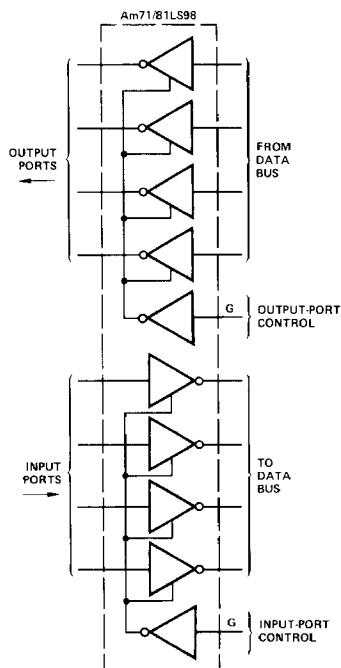
## APPLICATIONS

## Am71/81LS96 USED AS SYSTEM AND/OR MEMORY BUS DRIVER



LIC-497

## INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



LIC-498

## ORDERING INFORMATION

Package Type	Temperature Range	Order Number			
		Am71/81LS95	Am71/81LS96	Am71/81LS97	Am71/81LS98
Molded DIP	0°C to +70°C	DM81LS95N	DM81LS96N	DM81LS97N	DM81LS98N
Hermetic DIP	0°C to +70°C	DM81LS95J	DM81LS96J	DM81LS97J	DM81LS98J
Hermetic DIP	-55°C to +125°C	DM71LS95J	DM71LS96J	DM71LS97J	DM71LS98J
Dice	0°C to +70°C	AM81LS95X	AM81LS96X	AM81LS97X	AM81LS98X